

## CLAIMS

What is claimed is:

1. A method of performing model to hardware correlation, comprising:
  - simulating models based upon design criteria;
  - manufacturing devices based upon said design criteria;
  - evaluating features of said devices during said manufacturing to produce in-line test parametric data;
  - comparing said models to said in-line test parametric data to obtain correlation data; and
  - modifying said simulating according to said correlation data.
2. The method in claim 1, wherein said simulating produces geometric, DC, AC, and delay stage simulated parameters, and
  - wherein said in-line test parametric data includes geometric, DC, AC, and delay stage test parameters.
3. The method in claim 1, wherein said modifying produces a modified simulation and said method further comprises identifying, in a characterization map, ones of said devices that match models produced by said modified simulation.
4. The method in claim 1, wherein:
  - said devices comprise semiconductor devices;

3           said models include modeled threshold voltage values;  
4           said in-line test parametric data includes test threshold voltage values;  
5           said comparing compares said modeled threshold voltage values and said test threshold  
6 voltage values to produce a threshold voltage adder; and  
7           said modifying includes adding said threshold voltage adder to said modeled threshold  
8 voltage values.

1       5.     The method in claim 1, wherein:  
2           said devices comprise semiconductor devices;  
3           said models include modeled saturated current values;  
4           said in-line test parametric data includes test saturated current values;  
5           said comparing compares said modeled saturated current values and said test saturation  
6 saturated current values to produce a saturated current error value.

1       6.     The method in claim 1, wherein:  
2           said devices comprise semiconductor devices;  
3           said models include modeled delay per stage values;  
4           said in-line test parametric data includes test delay per stage values;  
5           said comparing compares said modeled delay per stage values and said test saturation  
6 delay per stage values to produce a delay per stage error value.

1 7. The method in claim 1, further comprising culling said in-line test parametric data to  
2 retain selected geometric, D.C., A.C. and delay test parameters.

1 8. The method in claim 1, further comprising identifying defective devices and removing  
2 said defective devices from said in-line test parametric data.

1 9. A method of correcting a hardware modeling process, said method comprising:  
2 manufacturing devices based on design criteria;  
3 measuring features of said devices to produce measured features;  
4 isolating a portion of said modeling process;  
5 supplying at least one of said measured features to said portion of said modeling process,  
6 wherein said portion of said modeling process outputs a simulated result;  
7 comparing said simulated result to a corresponding measured feature of said measured  
8 features; and  
9 calculating a correction to said portion of said modeling process based on said comparing.

1 10. The method in claim 9, wherein said simulated result and said corresponding measured  
2 feature comprise one of a voltage, current, and physical dimension.

1 11. The method in claim 9, wherein said portion of said modeling process simulates an  
2 integrated circuit design to model one of saturation threshold voltage, saturated source/drain  
3 current, and delay per stage.

1 12. The method in claim 9, further comprising repeating said method for second portions of  
2 said modeling process to produce second corrections.

1 13. The method in claim 12, further comprising modifying said modeling process based on  
2 said correction and said second corrections, such that said modeling process automatically makes  
3 said corrections after performing a simulation.

1 14. The method in claim 9, wherein said measuring comprises measuring physical  
2 dimensions and performance operations of said devices at different points of said manufacturing  
3 of said devices.

1 15. The method in claim 9, further comprising performing a statistical analysis based on  
2 results of said comparing process.

1 16. A method of performing model to hardware correlation for semiconductor chips,  
2 comprising:  
3 obtaining fabrication in-line parametric data;  
4 extracting first parameters from said parametric data to make a first set of go-data;  
5 calculating a first simulated threshold voltage saturation and first simulated saturated  
6 source/drain current based on said first set of go-data using a modeling program;

7 performing a first comparing of said first simulated threshold voltage saturation to an in-  
8 line parametric threshold voltage saturation from said parametric data and a first comparing of  
9 said first simulated saturated source/drain current to an in-line parametric saturated source/drain  
10 current from said parametric data;

11 calculating a threshold voltage adder from said first comparing; and

12 correcting said modeling program using said threshold voltage adder.

1 17. The method in claim 16, further comprising

2 adding said threshold voltage adder to said first set of go-data to make a second set of go-  
3 data;

4 calculating a second simulated threshold voltage saturation and second simulated  
5 saturated source/drain current based on said second set of go-data using said modeling program;

6 performing a second comparing of said second simulated threshold voltage saturation to  
7 said in-line parametric threshold voltage saturation and a second comparing of said second  
8 simulated saturated source/drain current to said in-line parametric saturated source/drain current;  
9 and

10 verifying that said threshold voltage adder corrected said second simulated threshold  
11 voltage saturation and said second simulated saturated source/drain current.

1 18. The method in claim 17, further comprising calculating a percentage error based on said  
2 second comparing process and adding said percentage error to said second set of go-data to make  
3 a third set of go-data.

1 19. The method in claim 18, further comprising:  
2 calculating a simulated delay-per-stage based on said third set of go-data using said  
3 modeling program;  
4 performing a third comparing of said simulated delay-per-stage to an in-line parametric  
5 delay-per-stage from said parametric data; and  
6 calculating a delay-per-stage error based on said third comparing process.

1 20. The method in claim 19, further comprising:  
2 adding said delay-per-stage error to said third set of go-data to make a final set of go-  
3 data; and  
4 outputting statistics based on said threshold voltage adder, said percentage error and said  
5 delay-per-stage error.

1 21. The method in claim 18, further comprising:  
2 performing a fourth comparing of parametric yield data from said final set of go-data to  
3 functional yield data from wafer final test servers;  
4 selecting acceptable chips which have good parametric yield data and good functional  
5 yield data from said fourth comparing process; and  
6 creating a model to hardware wafer map showing locations of said acceptable chips.

1 22. The method in claim 21, further comprising performing a model to hardware comparison  
2 using said model to hardware wafer map.

1 23. The method in claim 16, further comprising, after said extracting, removing defective  
2 chips from said first parameters to make said first set of go-data.

1 24. A method of performing model to hardware correlation for semiconductor chips,  
2 comprising:

3 obtaining fabrication in-line parametric data;

4 extracting first parameters from said parametric data to make a first set of go-data;

5 calculating a first simulated threshold voltage saturation and first simulated saturated  
6 source/drain current based on said first set of go-data using a modeling program;

7 performing a first comparing of said first simulated threshold voltage saturation to an in-  
8 line parametric threshold voltage saturation from said parametric data and a first comparing of  
9 said first simulated saturated source/drain current to an in-line parametric saturated source/drain  
10 current from said parametric data;

11 calculating a threshold voltage adder from said first comparing;

12 adding said threshold voltage adder to said first set of go-data to make a second set of go-  
13 data;

14 calculating a second simulated threshold voltage saturation and second simulated  
15 saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current; calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data; calculating a simulated delay-per-stage based on said third set of go-data using said modeling program; performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data; calculating a delay-per-stage error based on said third comparing process; adding said delay-per-stage error to said third set of go-data to make a final set of go-data; and correcting said modeling program using said final set of go-data.

25. The method in claim 24, further comprising, after said extracting, removing defective chips from said first parameters to make said first set of go-data.

26. The method in claim 24, further comprising, after said second comparing, verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current.



1 27. The method in claim 24, further comprising outputting statistics based on said threshold  
2 voltage adder, said percentage error and said delay-per-stage error.

1 28. The method in claim 24, further comprising:  
2 performing a fourth comparing of parametric yield data from said final set of go-data to  
3 functional yield data from wafer final test servers;  
4 selecting acceptable chips which have good parametric yield data and good functional  
5 yield data from said fourth comparing process;  
6 creating a model to hardware wafer map showing locations of said acceptable chips; and  
7 performing a model to hardware comparison using said model to hardware wafer map.

1 29. A method of performing model to hardware correlation for semiconductor chips,  
2 comprising:  
3 obtaining fabrication line parametric data;  
4 extracting first parameters from said parametric data;  
5 removing defective chips from said first parameters to make a first set of go-data;  
6 calculating a first simulated threshold voltage saturation and first simulated saturated  
7 source/drain current based on said first set of go-data using a modeling program;  
8 performing a first comparing of said first simulated threshold voltage saturation to an in-  
9 line parametric threshold voltage saturation from said parametric data and a first comparing of  
10 said first simulated saturated source/drain current to an in-line parametric saturated source/drain  
11 current from said parametric data;

calculating a threshold voltage adder from said first comparing;

adding said threshold voltage adder to said first set of go-data to make a second set of go-data;

calculating a second simulated threshold voltage saturation and second simulated saturated source/drain current based on said second set of go-data using said modeling program;

performing a second comparing of said second simulated threshold voltage saturation to said in-line parametric threshold voltage saturation and a second comparing of said second simulated saturated source/drain current to said in-line parametric saturated source/drain current;

verifying that said threshold voltage adder corrected said second simulated threshold voltage saturation and said second simulated saturated source/drain current;

calculating a percentage error based on said second comparing process and adding said percentage error to said second set of go-data to make a third set of go-data;

calculating a simulated delay-per-stage based on said third set of go-data using said modeling program;

performing a third comparing of said simulated delay-per-stage to an in-line parametric delay-per-stage from said parametric data;

calculating a delay-per-stage error based on said third comparing process;

adding said delay-per-stage error to said third set of go-data to make a final set of go-data;

outputting statistics based on said threshold voltage adder, said percentage error and said delay-per-stage error;

33 performing a fourth comparing of parametric yield data from said final set of go-data to  
34 functional yield data from wafer final test servers;  
35 selecting acceptable chips which have good parametric yield data and good functional  
36 yield data from said fourth comparing process;  
37 creating a model to hardware wafer map showing locations of said acceptable chips; and  
38 performing a model to hardware comparison using said model to hardware wafer map.

1 30. A program storage device readable by machine, tangibly embodying a program of  
2 instructions executable by the machine to perform method steps for performing model to  
3 hardware correlation, comprising:  
4 simulating models based upon design criteria;  
5 manufacturing devices based upon said design criteria;  
6 evaluating features of said devices during said manufacturing to produce in-line test  
7 parametric data;  
8 comparing said models to said in-line test parametric data to obtain correlation data; and  
9 modifying said simulating according to said correlation data.

1 31. The program storage device as claimed in claim 30, wherein said simulating produces  
2 geometric, DC, AC, and delay stage simulated parameters, and  
3 wherein said in-line test parametric data includes geometric, DC, AC, and delay stage test  
4 parameters.

1 32. The program storage device as claimed in claim 30, wherein said modifying produces a  
2 modified simulation and said method further comprises identifying, in a characterization map,  
3 ones of said devices that match models produced by said modified simulation.

1 33. The program storage device as claimed method in claim 30, wherein:  
2 said devices comprise semiconductor devices;  
3 said models include modeled threshold voltage values;  
4 said in-line test parametric data includes test threshold voltage values;  
5 said comparing compares said modeled threshold voltage values and said test threshold  
6 voltage values to produce a threshold voltage adder; and  
7 said modifying includes adding said threshold voltage adder to said modeled threshold  
8 voltage values.

1 34. The program storage device as claimed method in claim 30, wherein:  
2 said devices comprise semiconductor devices;  
3 said models include modeled saturated current values;  
4 said in-line test parametric data includes test saturated current values;  
5 said comparing compares said modeled saturated current values and said test saturation  
6 saturated current values to produce a saturated current error value.

1 35. The program storage device as claimed method in claim 30, wherein:  
2 said devices comprise semiconductor devices;

said models include modeled delay per stage values;

said in-line test parametric data includes test delay per stage values;

said comparing compares said modeled delay per stage values and said test saturation

delay per stage values to produce a delay per stage error value.

36. The program storage device as claimed method in claim 30, further comprising culling

said in-line test parametric data to retain selected geometric, D.C., A.C. and delay test

parameters.